8-Pin, 24-Bit, 96 kHz Stereo D/A Converter

Features

- Complete Stereo DAC System: Interpolation, D/A, Output Analog Filtering
- 24-Bit Conversion
- 96 dB Dynamic Range
- Low Distortion
- Low Clock Jitter Sensitivity
- Single +5 V Power Supply
- Filtered Line Level Outputs
- On-Chip Digital De-emphasis
- Soft Ramp to Quiescent Output Voltage
- Functionally Compatibile with CS4330/31/33

Description

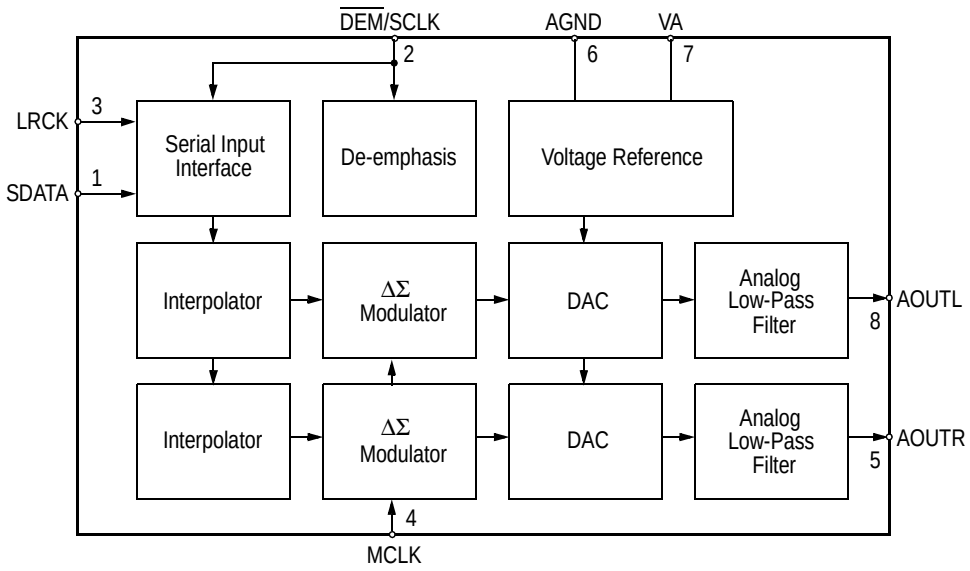
The CS4334 family members are complete, stereo digital-to-analog output systems including interpolation, 1-bit D/A conversion and output analog filtering in an 8-pin package. The CS4334/5/6/7/8/9 support all major audio data interface formats and the individual devices differ only in the supported interface format.

The CS4334 family is based on delta-sigma modulation, where the modulator output controls the reference voltage input to an ultra-linear analog low-pass filter. This architecture allows for infinite adjustment of sample rate between 2 kHz and 100 kHz simply by changing the master clock frequency.

The CS4334 family contains on-chip digital de-emphasis, operates from a single +5V power supply, and requires minimal support circuitry. These features are ideal for portable CD players and other portable playback systems.

ORDERING INFORMATION

See page 20



Preliminary Product Information | This document contains information for a new product. Cirrus Logic reserves the right to modify this product without notice.

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ANALOG CHARACTERISTICS (T_A = 25 °C; Logic "1" = VA = 5 V; Logic "0" = AGND;

Full-Scale Output Sine Wave, 997 Hz; MCLK = 12.288 MHz; Fs for Base-rate Mode = 48 kHz, SCLK = 3.072 MHz, Measurement Bandwidth 10 Hz to 20 kHz, unless otherwise specified; Fs for High-Rate Mode = 96 kHz, SCLK = 6.144 MHz, Measurement Bandwidth 10 Hz to 40 kHz, unless otherwise specified. Test load R_L = 10 kΩ, C_L = 10 pF (see Figure 1))

Parameter			Symbol	Base-rate Mode Min	Base-rate Mode Typ	Base-rate Mode Max	High-Rate Mode Min	High-Rate Mode Typ	High-Rate Mode Max	Unit
Dynamic Performance for CS4334/5/6/7/8/9-KS										
Specified Temperature Range			T_A	-10	-	70	-10	-	70	°C
Dynamic Range		(Note 1)								
	18 to 24-Bit	unweighted		TBD	93	-	TBD	90	-	dB
		A-Weighted		TBD	96	-	TBD	96	-	dB
	16-Bit	unweighted		TBD	91	-	TBD	88	-	dB
		A-Weighted		TBD	94	-	TBD	94	-	dB
Total Harmonic Distortion + Noise		(Note 1)	THD+N							
	18 to 24-Bit	0 dB		-	-88	TBD	-	-88	TBD	dB
		-20 dB		-	-73	TBD	-	-70	TBD	dB
		-60 dB		-	-33	TBD	-	-30	TBD	dB
	16-Bit	0 dB		-	-86	TBD	-	-86	TBD	dB
		-20 dB		-	-71	TBD	-	-68	TBD	dB
		-60 dB		-	-31	TBD	-	-28	TBD	dB
Interchannel Isolation		(1 kHz)		-	90	-	-	90	-	dB
Dynamic Performance for CS4334/5/6/7/8/9-BS										
Specified Temperature Range			T_A	-40	-	85	-40	-	85	°C
Dynamic Range		(Note 1)								
	18 to 24-Bit	unweighted		TBD	93	-	TBD	90	-	dB
		A-Weighted		TBD	96	-	TBD	96	-	dB
	16-Bit	unweighted		TBD	91	-	TBD	88	-	dB
		A-Weighted		TBD	94	-	TBD	94	-	dB
Total Harmonic Distortion + Noise		(Note 1)	THD+N							
	18 to 24-Bit	0 dB		-	-88	TBD	-	-88	TBD	dB
		-20 dB		-	-73	TBD	-	-70	TBD	dB
		-60 dB		-	-33	TBD	-	-30	TBD	dB
	16-Bit	0 dB		-	-86	TBD	-	-86	TBD	dB
		-20 dB		-	-71	TBD	-	-68	TBD	dB
		-60 dB		-	-31	TBD	-	-28	TBD	dB
Interchannel Isolation		(1 kHz)		-	90	-	-	90	-	dB

Notes: 1. Triangular PDF dithered data.

ANALOG CHARACTERISTICS (Continued)

Parameter	Symbol	Base-rate Mode Min	Base-rate Mode Typ	Base-rate Mode Max	High-Rate Mode Min	High-Rate Mode Typ	High-Rate Mode Max	Unit
Combined Digital and On-chip Analog Filter Response								
Passband (Note 2)								
to -0.05 dB corner		0	-	.4535	-	-	-	Fs
to -0.1 dB corner		-	-	-	0	-	.4621	Fs
to -3 dB corner		0	-	TBD	0	-	TBD	Fs
Frequency Response 10 Hz to 20 kHz		-.02	-	+.035	-0.1	-	0	dB
Passband Ripple		-	-	±.035	-	-	±.13	dB
StopBand		.5465	-	-	.577	-	-	Fs
StopBand Attenuation (Note 3)		50	-	-	55	-	-	dB
Group Delay	tgd	-	9/Fs	-	-	9/Fs	-	s
Passband Group Delay Deviation 0 - 40 kHz		-	±0.36/Fs	-	-	±1.39/Fs	-	s
0 - 20 kHz					-	±0.23/Fs	-	s
De-emphasis Error (Fs = 44.1 kHz only)		-	-	TBD	-	-	TBD	dB

Parameters	Symbol	Min	Typ	Max	Units
dc Accuracy					
Interchannel Gain Mismatch		-	0.1	-	dB
Gain Error		-	±5	TBD	%
Gain Drift		-	100	-	ppm/°C
Analog Output					
Full Scale Output Voltage		TBD	3.4	TBD	Vpp
Quiescent Voltage	V_Q	-	2.2	-	VDC
AC-Load Resistance (Note 4)	R_L	3	-	-	kΩ
Load Capacitance (Note 4)	C_L	-	-	100	pF

Notes: 2. Response is clock dependent and will scale with Fs. Note that the response plots (Figures 13-20) have been normalized to Fs and can be de-normalized by multiplying the X-axis scale by Fs.

3. For Base-Rate Mode, the Measurement Bandwidth is 0.5465 Fs to 3 Fs.
For High-Rate Mode, the Measurement Bandwidth is 0.577 Fs to 1.4 Fs.

4. Refer to Figure 2.

POWER AND THERMAL CHARACTERISTICS

Parameters	Symbol	Base-rate Mode Min	Base-rate Mode Typ	Base-rate Mode Max	High-Rate Mode Min	High-Rate Mode Typ	High-Rate Mode Max	Units
Power Supplies								
Power Supply Current normal operation	I_A	-	15	TBD	-	15	TBD	mA
power-down state	I_A	-	60	-	-	60	-	µA
Power Dissipation (Note 5)								
normal operation		-	75	TBD	-	75	TBD	mW
power-down		-	0.3	-	-	0.3	-	mW
Package Thermal Resistance	θ_{JA}	-	110	-	-	110	-	°C/Watt
Power Supply Rejection Ratio (1 kHz)	PSRR	-	50	-	-	50	-	dB

Notes: 5. Refer to Figure 3.

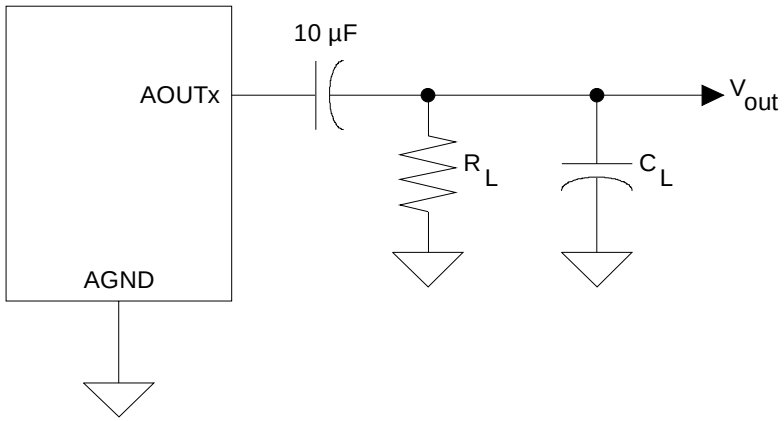


Figure 1. Output Test Load

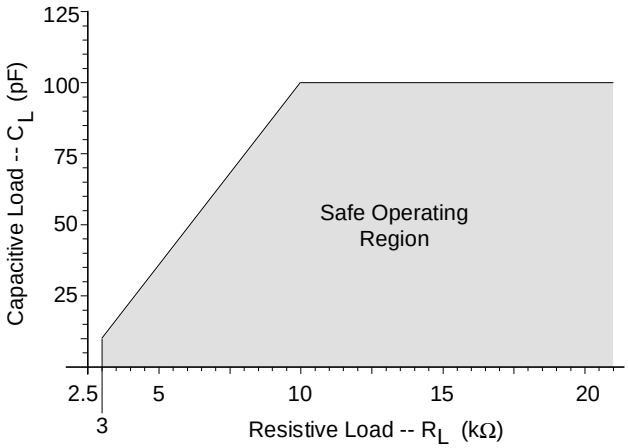


Figure 2. Maximum Loading

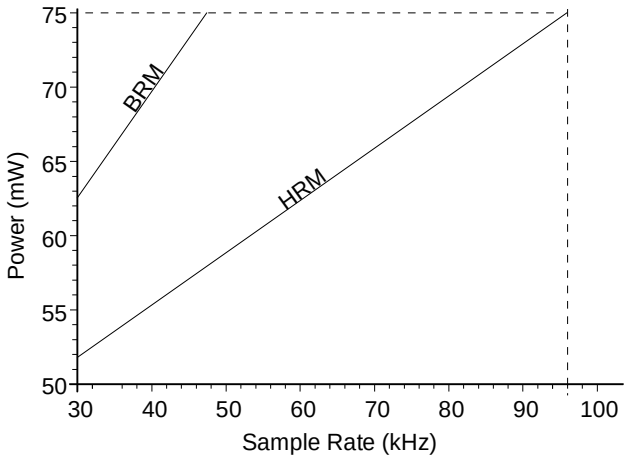


Figure 3. Power vs. Sample Rate

DIGITAL CHARACTERISTICS (T_A = 25°C; VA = 4.75V - 5.5V)

Parameters	Symbol	Min	Typ	Max	Units
High-Level Input Voltage	V_{IH}	2.0	-	-	V
Low-Level Input Voltage	V_{IL}	-	-	0.8	V
Input Leakage Current (Note 6)	I_{in}	-	-	±10	µA
Input Capacitance		-	8	-	pF

Notes: 6. I_{in} for CS433X LRCK is ±20µA max.

ABSOLUTE MAXIMUM RATINGS (AGND = 0V; all voltages with respect to ground.)

Parameters	Symbol	Min	Max	Units
DC Power Supply	VA	-0.3	6.0	V
Input Current, Any Pin Except Supplies	I_{in}	-	±10	mA
Digital Input Voltage	V_{IND}	-0.3	VA+0.4	V
Ambient Operating Temperature (power applied)	T_A	-55	125	°C
Storage Temperature	T_{stg}	-65	150	°C

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS (AGND = 0V; all voltages with respect to ground.)

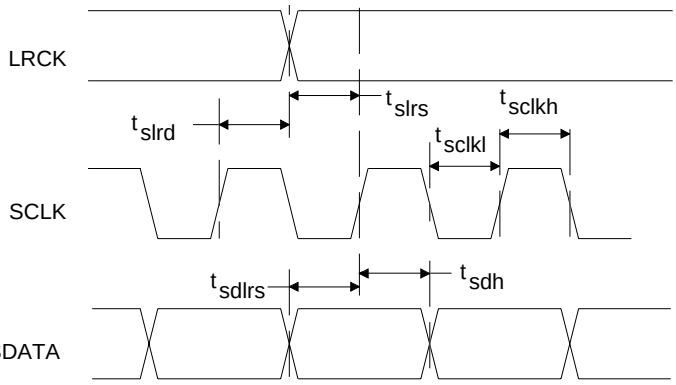
Parameters	Symbol	Min	Typ	Max	Units
DC Power Supply	VA	4.75	5.0	5.5	V

SWITCHING CHARACTERISTICS (T_A = -40 to 85°C; VA = 4.75V - 5.5V; Inputs: Logic 0 = 0V, Logic 1 = VA, CL = 20pF)

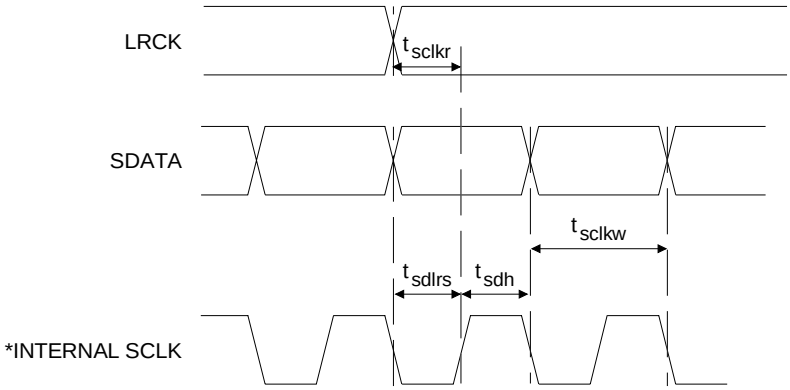
Parameters	Symbol	Min	Typ	Max	Units
Input Sample Rate	Fs	2	-	100	kHz
MCLK Pulse Width High MCLK/LRCK = 512		10	-	1000	ns
MCLK Pulse Width Low MCLK/LRCK = 512		10	-	1000	ns
MCLK Pulse Width High MCLK / LRCK = 384 or 192		21	-	1000	ns
MCLK Pulse Width Low MCLK / LRCK = 384 or 192		21	-	1000	ns
MCLK Pulse Width High MCLK / LRCK = 256 or 128		31	-	1000	ns
MCLK Pulse Width Low MCLK / LRCK = 256 or 128		31	-	1000	ns
External SCLK Mode					
LRCK Duty Cycle (External SCLK only)		40	50	60	%
SCLK Pulse Width Low	t_{sclkl}	20	-	-	ns
SCLK Pulse Width High	t_{sclkh}	20	-	-	ns
SCLK Period MCLK / LRCK = 512, 256 or 384	t_{sclkw}	$\frac{1}{(128)Fs}$	-	-	ns
SCLK Period MCLK / LRCK = 128 or 192	t_{sclkw}	$\frac{1}{(64)Fs}$	-	-	ns
SCLK rising to LRCK edge delay	t_{slrd}	20	-	-	ns
SCLK rising to LRCK edge setup time	t_{slrs}	20	-	-	ns
SDATA valid to SCLK rising setup time	t_{sdlrs}	20	-	-	ns
SCLK rising to SDATA hold time	t_{sdh}	20	-	-	ns
Internal SCLK Mode					
LRCK Duty Cycle (Internal SCLK only) (Note 7)		-	50	-	%
SCLK Period (Note 8)	t_{sclkw}	$\frac{1}{SCLK}$	-	-	ns
SCLK rising to LRCK edge	t_{sclkr}	-	$\frac{tsclkw}{2}$	-	µs
SDATA valid to SCLK rising setup time	t_{sdlrs}	$\frac{1}{(512)Fs} + 10$	-	-	ns
SCLK rising to SDATA hold time MCLK / LRCK = 512, 256 or 128	t_{sdh}	$\frac{1}{(512)Fs} + 15$	-	-	ns
SCLK rising to SDATA hold time MCLK / LRCK = 384 or 192	t_{sdh}	$\frac{1}{(384)Fs} + 15$	-	-	ns

Notes: 7. In Internal SCLK Mode, the Duty Cycle must be 50% +/– 1/2 MCLK Period.

8. The SCLK / LRCK ratio may be either 32, 48, or 64. This ratio depends on part type and MCLK/LRCK ratio. (See figures 7-12)

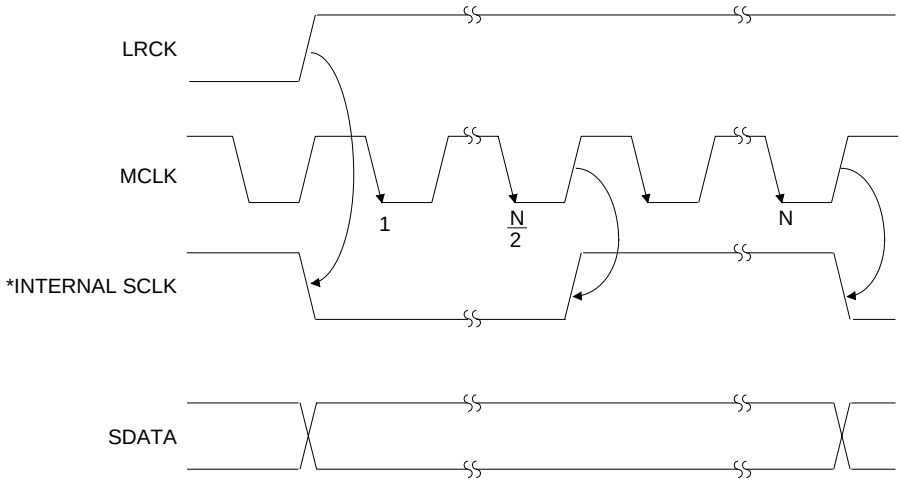


External Serial Mode Input Timing



Internal Serial Mode Input Timing

* The SCLK pulses shown are internal to the CS4334/5/6/7/8/9.



Internal Serial Clock Generation

* The SCLK pulses shown are internal to the CS4334/5/6/7/8/9.

N equals MCLK divided by SCLK

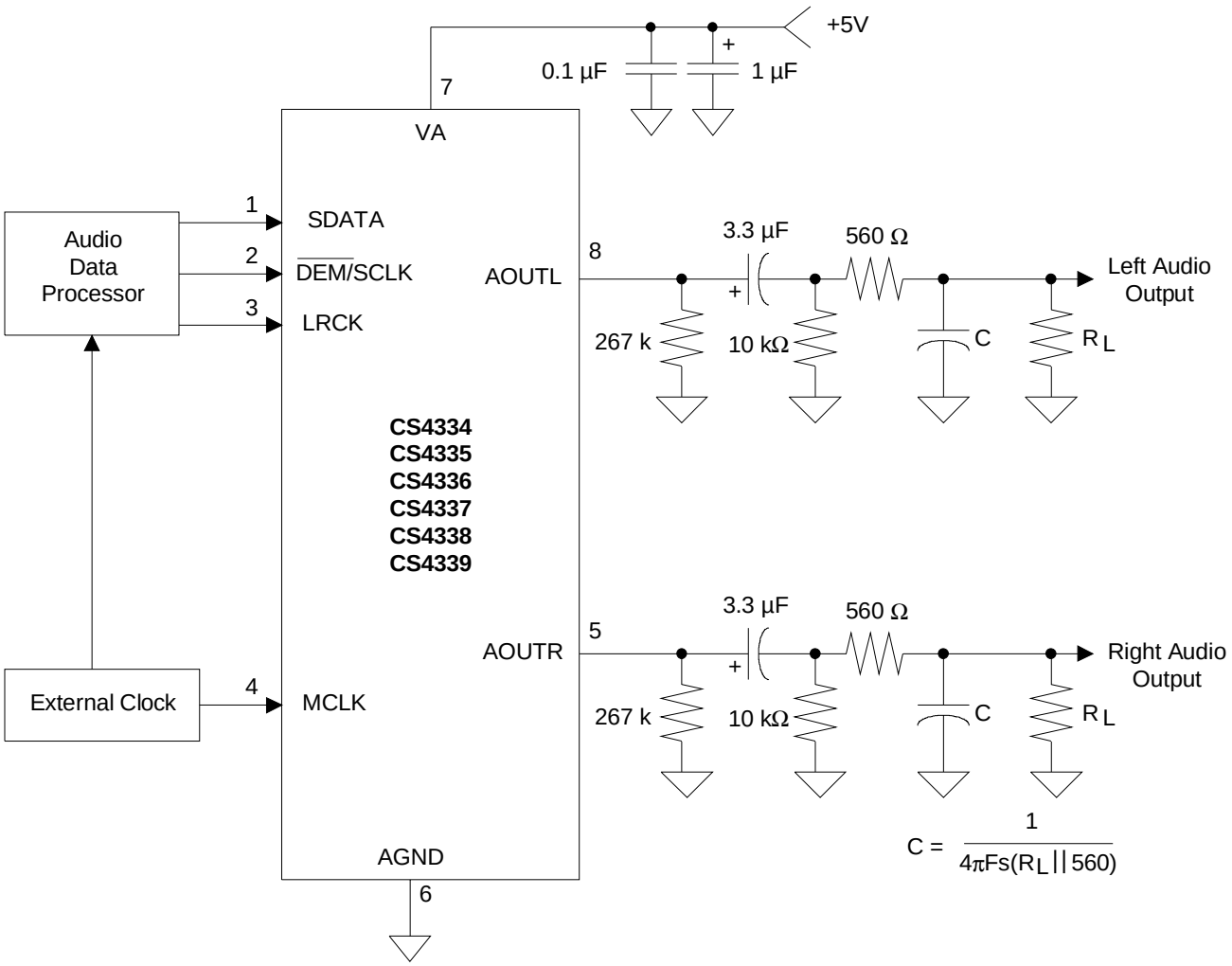


Figure 4. Recommended Connection Diagram

GENERAL DESCRIPTION

The CS4334 family of devices offers a complete stereo digital-to-analog system including digital interpolation, fourth-order delta-sigma digital-to-analog conversion, digital de-emphasis and analog filtering, as shown in Figure 5. This architecture provides a high tolerance to clock jitter.

The primary purpose of using delta-sigma modulation techniques is to avoid the limitations of laser trimmed resistive digital-to-analog converter architectures by using an inherently linear 1-bit digital-to-analog converter. The advantages of a 1-bit digital-to-analog converter include: ideal differential linearity, no distortion mechanisms due to resistor matching errors and no linearity drift over time and temperature due to variations in resistor values.

The CS4334 family of devices supports two modes of operation. The devices operate in Base Rate Mode (BRM) when MCLK/LRCK is 256, 384 or 512 and in High Rate Mode (HRM) when MCLK/LRCK is 128 or 192. High Rate Mode allows input sample rates up to 100 kHz.

Digital Interpolation Filter

The digital interpolation filter increases the sample rate, Fs, by a factor of 4 and is followed by a 32× digital sample-and-hold (16× in HRM). This filter eliminates images of the baseband audio signal which exist at multiples of the input sample rate. The resulting frequency spectrum has images of the input signal at multiples of 4 Fs. These images are easily removed by the on-chip analog low-pass filter and a simple external analog filter (see Figure 4).

Delta-Sigma Modulator

The interpolation filter is followed by a fourth order delta-sigma modulator which converts the interpolation filter output into 1-bit data at a rate of 128 Fs in BRM (or 64 Fs in HRM).

Switched-Capacitor DAC

The delta-sigma modulator is followed by a digital-to-analog converter which translates the 1-bit data into a series of charge packets. The magnitude of the charge in each packet is determined by sampling of a voltage reference onto a switched capacitor, where the polarity of each packet is controlled by the 1-bit data. This technique greatly reduces the sensitivity to clock jitter and provides low-pass filtering of the output.

Analog Low-Pass Filter

The final signal stage consists of a continuous-time low-pass filter which serves to smooth the output and attenuate out-of-band noise.

SYSTEM DESIGN

The CS4334 family accepts data at standard audio sample rates including 48, 44.1 and 32 kHz in BRM and 96, 88.2 and 64 kHz in HRM. Audio data is input via the serial data input pin (SDATA). The Left/Right Clock (LRCK) defines the channel and delineation of data, and the Serial Clock (SCLK) clocks audio data into the input data buffer. The CS4334/5/6/7/8/9 differ in serial data formats as shown in Figures 7-12.

Master Clock

MCLK must be either 256x, 384x or 512x the desired input sample rate in BRM and either 128x or

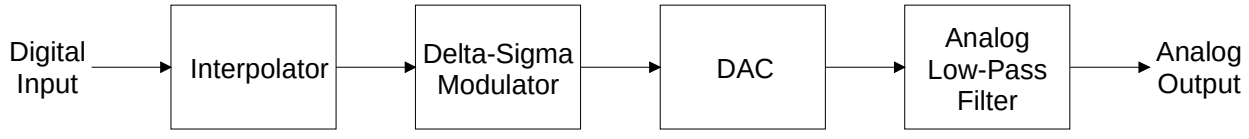


Figure 5. System Block Diagram

192x the desired input sample rate in HRM. The LRCK frequency is equal to Fs, the frequency at which words for each channel are input to the device. The MCLK-to-LRCK frequency ratio is detected automatically during the initialization sequence by counting the number of MCLK transitions during a single LRCK period. Internal dividers are set to generate the proper clocks. Table 1 illustrates several standard audio sample rates and the required MCLK and LRCK frequencies.

LRCK (kHz)	MCLK (MHz)				
	HRM		BRM		
	128x	192x	256x	384x	512x
32	4.0960	6.1440	8.1920	12.2880	16.3840
44.1	5.6448	8.4672	11.2896	16.9344	22.5792
48	6.1440	9.2160	12.2880	18.4320	24.5760
64	8.1920	12.2880	-	-	-
88.2	11.2896	16.9344	-	-	-
96	12.2880	18.4320	-	-	-

Table 1. Common Clock Frequencies

Serial Clock

The serial clock controls the shifting of data into the input data buffers. The CS4334 family supports both external and internal serial clock generation modes. Refer to Figures 7-12 for data formats.

External Serial Clock Mode

The CS4334 family will enter the External Serial Clock Mode when 16 low to high transitions are detected on the DEM/SCLK pin during any phase of the LRCK period. When this mode is enabled, the Internal Serial Clock Mode and de-emphasis filter cannot be accessed. The CS4334 family will switch to Internal Serial Clock Mode if no low to high transitions are detected on the DEM/SCLK pin for 2 consecutive frames of LRCK. Refer to Figure 21.

Internal Serial Clock Mode

In the Internal Serial Clock Mode, the serial clock is internally derived and synchronous with MCLK and LRCK. The SCLK/LRCK frequency ratio is either 32, 48, or 64 depending upon data format. Operation in this mode is identical to operation with an external serial clock synchronized with LRCK. This mode allows access to the digital de-emphasis function. Refer to Figures 7 - 21 for details.

While the Internal Serial Clock Mode is provided to allow access to the de-emphasis filter, the Internal Serial Clock Mode also eliminates possible clock interference from an external SCLK. Use of Internal Serial Clock Mode is always preferred, even when de-emphasis filtering is not required.

De-Emphasis

The CS4334 family includes on-chip digital de-emphasis. Figure 6 shows the de-emphasis curve for Fs equal to 44.1 kHz. The frequency response of the de-emphasis curve will scale proportionally with changes in sample rate, Fs.

The de-emphasis filter is active (inactive) if the DEM/SCLK pin is low (high) for 5 consecutive falling edges of LRCK. This function is available only in the internal serial clock mode.

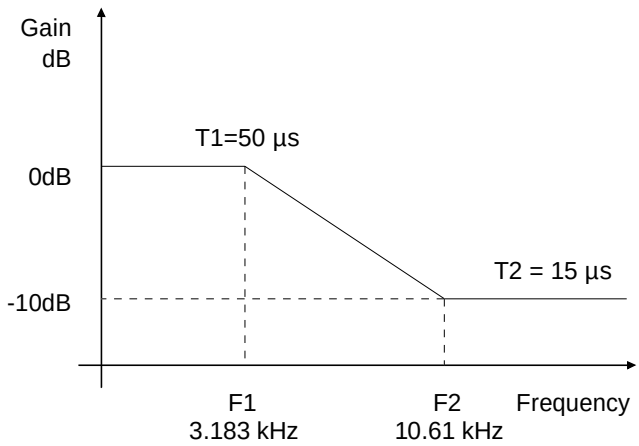


Figure 6. De-Emphasis Curve (Fs = 44.1kHz)

Initialization and Power-Down

The Initialization and Power-Down sequence flow chart is shown in Figure 21. The CS4334 family enters the Power-Down State upon initial power-up.

The interpolation filters and delta-sigma modulators are reset, and the internal voltage reference, one-bit digital-to-analog converters and switched-capacitor low-pass filters are powered down. The device will remain in the Power-Down mode until MCLK and LRCK are present. Once MCLK and LRCK are detected, MCLK occurrences are counted over one LRCK period to determine the MCLK/LRCK frequency ratio. Power is then applied to the internal voltage reference. Finally, power is applied to the D/A converters and switched-capacitor filters, and the analog outputs will ramp to the quiescent voltage, V_Q.

Output Transient Control

The CS4334 family uses a novel technique to minimize the effects of output transients during power-up and power-down. This technique, when used with external DC-blocking capacitors in series with the audio outputs, eliminates the audio transients commonly produced by single-ended single-supply converters. To make best use of this feature, it is necessary to understand its operation.

When the device is initially powered-up, the audio outputs, AOUTL and AOUTR, are clamped to AGND. After a short delay of approximately 1000 sample periods, each output begins to ramp towards its quiescent voltage, V_Q. Approximately 10,000 sample cycles later, the outputs reach V_Q and audio output begins. This gradual voltage ramping allows time for the external DC-blocking capacitor to charge to V_Q, effectively blocking the quiescent DC voltage.

To prevent transients at power-down, the device must first enter its power-down state. This is accomplished by removing MCLK or LRCK. When this occurs, audio output ceases and the internal output buffers are disconnected from AOUTL and AOUTR. In their place, a soft-start current sink is substituted which allows the DC-blocking capacitors to slowly discharge. Once this charge is dissipated, the power to the device may be turned off and the system is ready for the next power-on.

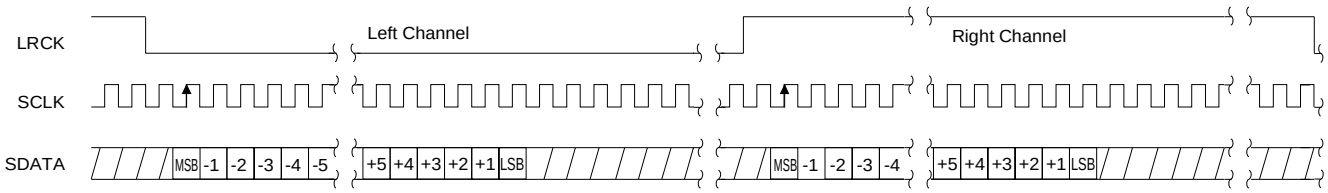
To prevent an audio transient at the next power-on, it is necessary to ensure that the DC-blocking capacitors have fully discharged before turning off the power or exiting the power-down state. If not, a transient will occur when the audio outputs are initially clamped to AGND. The time that the device must remain in the power-down state is related to the value of the DC-blocking capacitance. For example, with a 3.3 µF capacitor, the time that the device must remain in the power-down state will be approximately 0.4 seconds.

Grounding and Power Supply Decoupling

As with any high resolution converter, the CS4334 family requires careful attention to power supply and grounding arrangements to optimize performance. Figure 4 shows the recommended power arrangement with VA connected to a clean +5V supply. Decoupling capacitors should be located as close to the device package as possible.

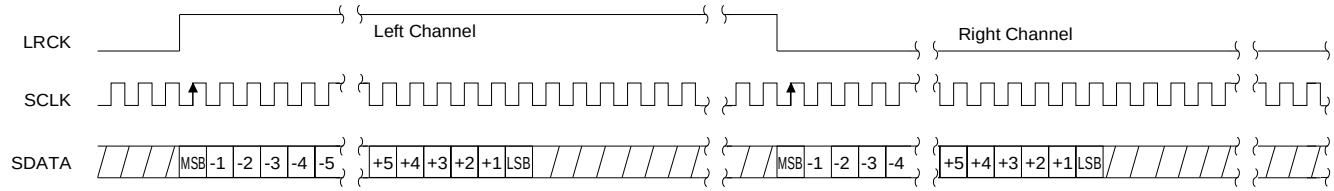
Analog Output and Filtering

The CS4334 family analog filter is a switched-capacitor filter followed by a continuous time low pass filter. Its response, combined with that of the digital interpolator, is given in Figures 13 - 20.



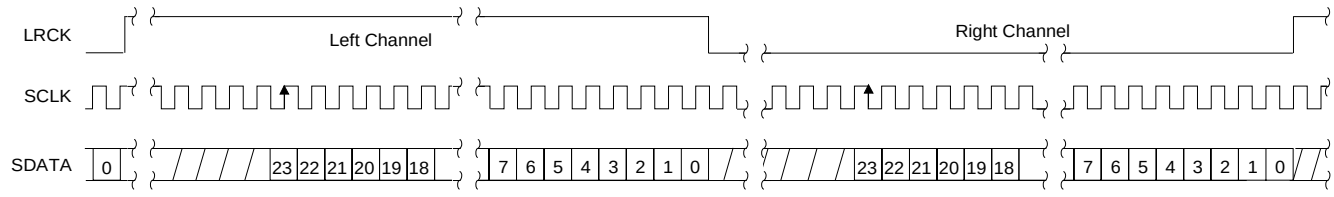
Internal SCLK Mode	External SCLK Mode
I^2S, 16-Bit data and INT SCLK = 32 Fs if MCLK/LRCK = 512, 256 or 128 I^2S, Up to 24-Bit data and INT SCLK = 48 Fs if MCLK/LRCK = 384 or 192	I^2S, up to 24-Bit Data Data Valid on Rising Edge of SCLK

Figure 7. CS4334 Data Format (I^2S)



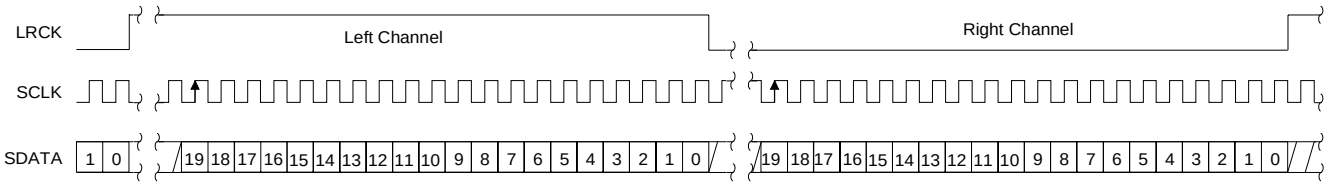
Internal SCLK Mode	External SCLK Mode
Left Justified, up to 24-Bit Data INT SCLK = 64 Fs if MCLK/LRCK = 512, 256 or 128 INT SCLK = 48 Fs if MCLK/LRCK = 384 or 192	Left Justified, up to 24-Bit Data Data Valid on Rising Edge of SCLK

Figure 8. CS4335 Data Format



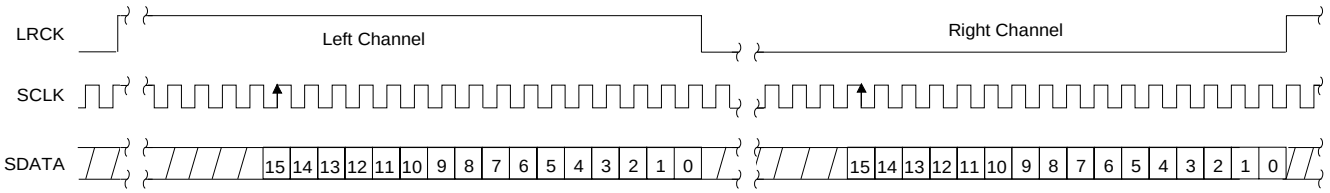
Internal SCLK Mode	External SCLK Mode
Right Justified, 24-Bit Data INT SCLK = 64 Fs if MCLK/LRCK = 512, 256 or 128 INT SCLK = 48 Fs if MCLK/LRCK = 384 or 192	Right Justified, 24-Bit Data Data Valid on Rising Edge of SCLK SCLK Must Have at Least 48 Cycles per LRCK Period

Figure 9. CS4336 Data Format



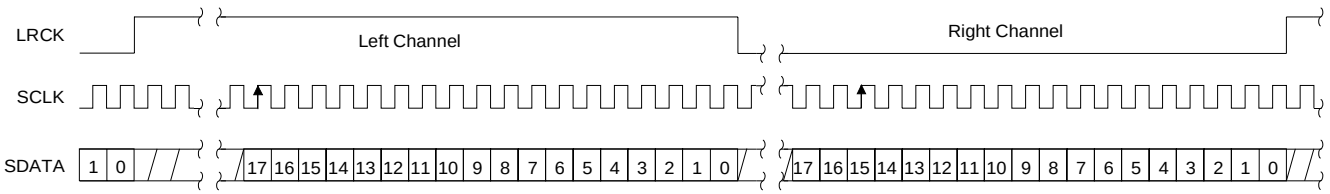
Internal SCLK Mode	External SCLK Mode
Right Justified, 20-Bit Data INT SCLK = 64 Fs if MCLK/LRCK = 512, 256 or 128 INT SCLK = 48 Fs if MCLK/LRCK = 384 or 192	Right Justified, 20-Bit Data Data Valid on Rising Edge of SCLK SCLK Must Have at Least 40 Cycles per LRCK Period

Figure 10. CS4337 Data Format



Internal SCLK Mode	External SCLK Mode
Right Justified, 16-Bit Data INT SCLK = 32 Fs if MCLK/LRCK = 512, 256 or 128 INT SCLK = 48 Fs if MCLK/LRCK = 384 or 192	Right Justified, 16-Bit Data Data Valid on Rising Edge of SCLK SCLK Must Have at Least 32 Cycles per LRCK Period

Figure 11. CS4338 Data Format



Internal SCLK Mode	External SCLK Mode
Right Justified, 18-Bit Data INT SCLK = 64 Fs if MCLK/LRCK = 512, 256 or 128 INT SCLK = 48 Fs if MCLK/LRCK = 384 or 192	Right Justified, 18-Bit Data Data Valid on Rising Edge of SCLK SCLK Must Have at Least 36 Cycles per LRCK Period

Figure 12. CS4339 Data Format

Overall Base-rate Frequency Response

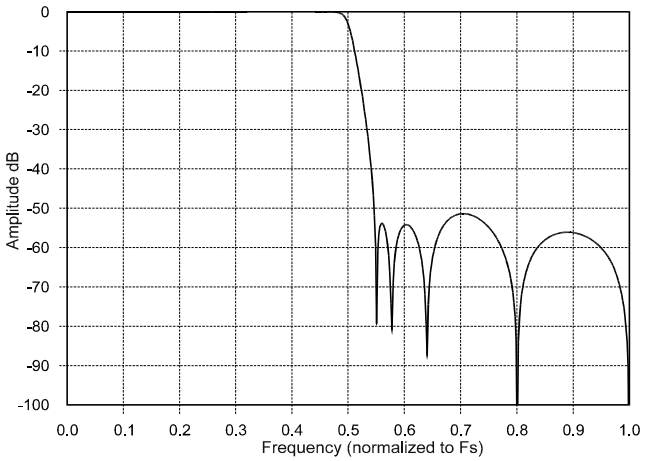


Figure 13. Stopband Rejection

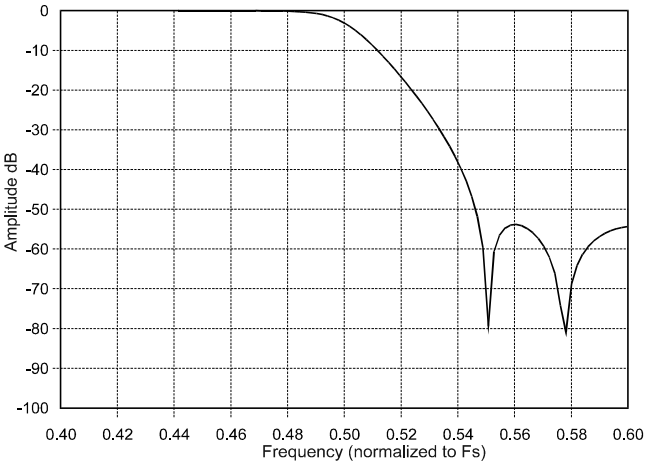


Figure 14. Transition Band

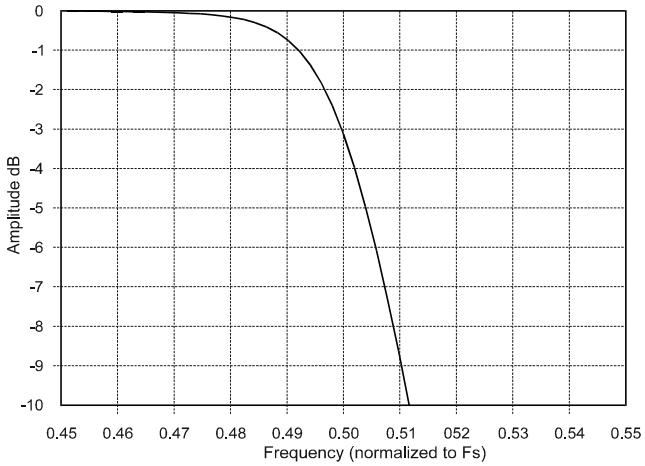


Figure 15. Transition Band

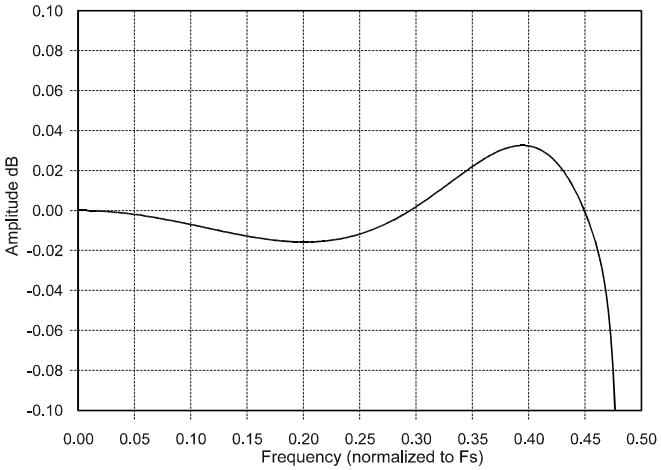


Figure 16. Passband Ripple

Overall High-rate Frequency Response

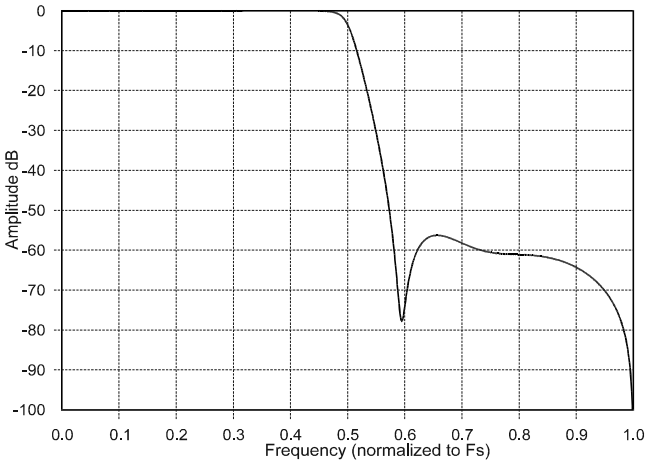


Figure 17. Stopband Rejection

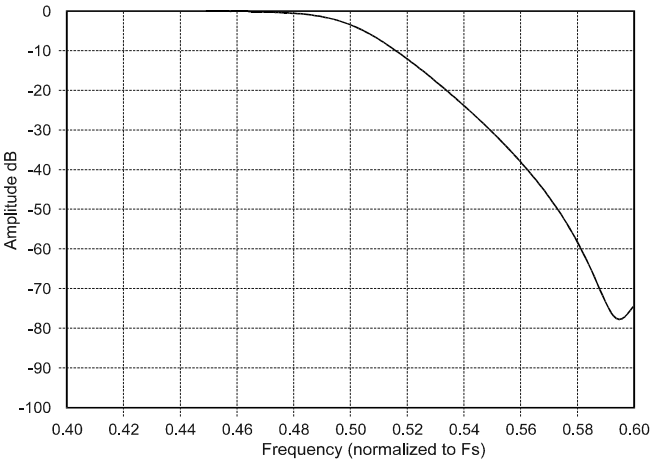


Figure 18. Transition Band

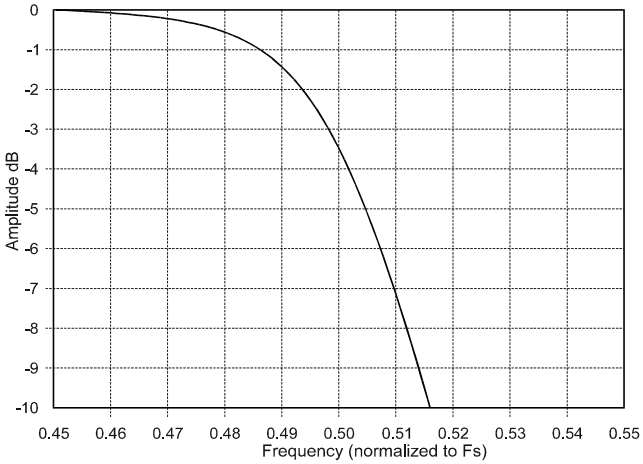


Figure 19. Transition Band

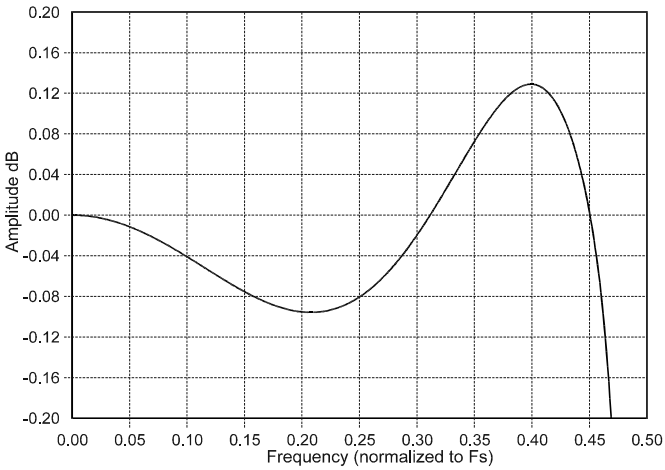


Figure 20. Passband Ripple

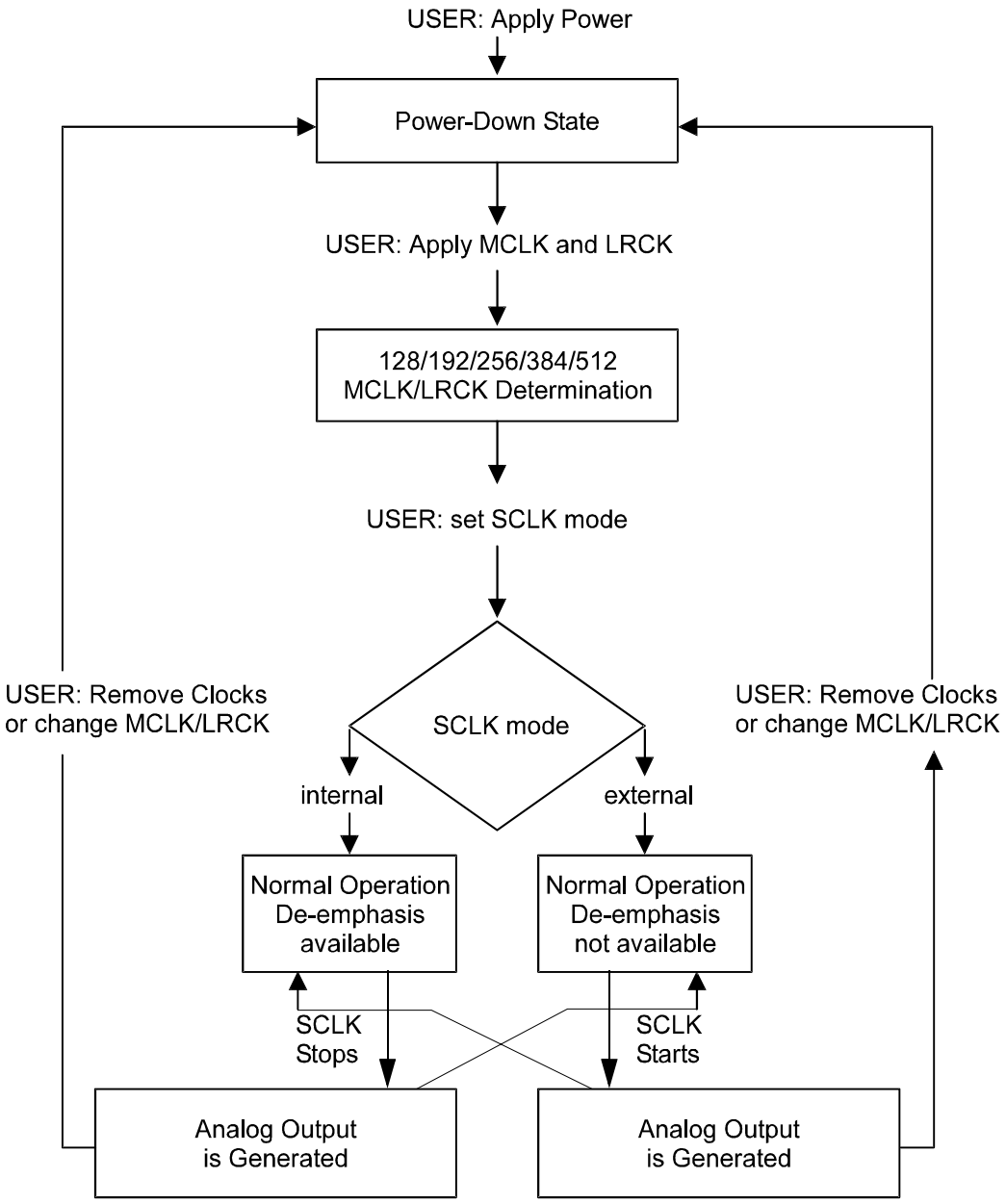


Figure 21. CS4334/5/6/7/8/9 Initialization and Power-Down Sequence

REFERENCES

1) "How to Achieve Optimum Performance from Delta-Sigma A/D & D/A Converters" by Steven Harris. Paper presented at the 93rd Convention of the Audio Engineering Society, October 1992.

2) CDB4334/5/6/7/8/9 Evaluation Board Datasheet

PIN DESCRIPTIONS

SERIAL DATA INPUT	**SDATA**	1	8	**AOUTL**	ANALOG LEFT CHANNEL OUTPUT
DE-EMPHASIS / SCLK	**DEM/SCLK**	2	7	**VA**	ANALOG POWER
LEFT / RIGHT CLOCK	**LRCK**	3	6	**AGND**	ANALOG GROUND
MASTER CLOCK	**MCLK**	4	5	**AOUTR**	ANALOG RIGHT CHANNEL OUTPUT

Power Supply Connections

VA - Analog Power, PIN 7.

Analog supply. Nominally +5V.

AGND - Analog Ground, PIN 6.

Analog ground reference.

Analog Outputs

AOUTL - Analog Left Channel Output, PIN 8.

Analog output for the left channel. Typically 3.5 Vpp for a full-scale input signal.

AOUTR - Analog Right Channel Output, PIN 5.

Analog output for the right channel. Typically 3.5 Vpp for a full-scale input signal.

Digital Inputs

MCLK - Master Clock Input, PIN 4.

The frequency must be 256x, 384x or 512x the input sample rate in Base Rate Mode (BRM) and either 128x or 192x the input sample rate in High Rate Mode (HRM).

LRCK - Left/Right Clock, PIN 3.

This input determines which channel is currently being input on the Audio Serial Data Input pin, SDATA.

SDATA - Audio Serial Data Input, PIN 1.

Two's complement MSB-first serial data is input on this pin. The data is clocked into the CS4334/5/6/7/8/9 via internal or external SCLK and the channel is determined by LRCK.

$\overline{\text{DEM}}$/SCLK - De-emphasis / External serial clock input , PIN 2.

A dual-purpose input used for de-emphasis filter control or external serial clock input.

PARAMETER DEFINITIONS

Total Harmonic Distortion + Noise (THD+N)- The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified bandwidth (typically 10Hz to 20kHz), including distortion components. Expressed in decibels.

Dynamic Range - The ratio of the full scale rms value of the signal to the rms sum of all other spectral components over the specified bandwidth. Dynamic range is a signal-to-noise measurement over the specified bandwidth made with a -60 dBFS signal. 60 dB is then added to the resulting measurement to refer the measurement to full scale. This technique ensures that the distortion components are below the noise level and do not effect the measurement. This measurement technique has been accepted by the Audio Engineering Society, AES17-1991, and the Electronic Industries Association of Japan, EIAJ CP-307.

Interchannel Isolation - A measure of crosstalk between the left and right channels. Measured for each channel at the converter's output with all zeros to the input under test and a full-scale signal applied to the other channel. Units in decibels.

Interchannel Gain Mismatch - The gain difference between left and right channels. Units in decibels.

Gain Error - The deviation from the nominal full scale analog output for a full scale digital input.

Gain Drift - The change in gain value with temperature. Units in ppm/°C.

ORDERING INFORMATION:

Model	Temperature	Package	Serial Interface
CS4334-KS	-10 to +70 °C	8-pin Plastic SOIC	16 to 24-bit, I2S
CS4335-KS	-10 to +70 °C	8-pin Plastic SOIC	16 to 24-bit, left justified
CS4336-KS	-10 to +70 °C	8-pin Plastic SOIC	24-bit, right justified
CS4337-KS	-10 to +70 °C	8-pin Plastic SOIC	20-bit, right justified
CS4338-KS	-10 to +70 °C	8-pin Plastic SOIC	16-bit, right justified
CS4339-KS	-10 to +70 °C	8-pin Plastic SOIC	18-bit, right justified, 32 F_S Internal SCLK mode
CS4334-BS	-40 to +85 °C	8-pin Plastic SOIC	16 to 24-bit, I2S
CS4335-BS	-40 to +85 °C	8-pin Plastic SOIC	16 to 24-bit, left justified
CS4336-BS	-40 to +85 °C	8-pin Plastic SOIC	24-bit, right justified
CS4337-BS	-40 to +85 °C	8-pin Plastic SOIC	20-bit, right justified
CS4338-BS	-40 to +85 °C	8-pin Plastic SOIC	16-bit, right justified
CS4339-BS	-40 to +85 °C	8-pin Plastic SOIC	18-bit, right justified, 32 F_S Internal SCLK mode

FUNCTIONAL COMPATIBILITY

CS4330-KS ⇒ CS4339-KS

CS4331-KS ⇒ CS4334-KS

CS4333-KS ⇒ CS4338-KS

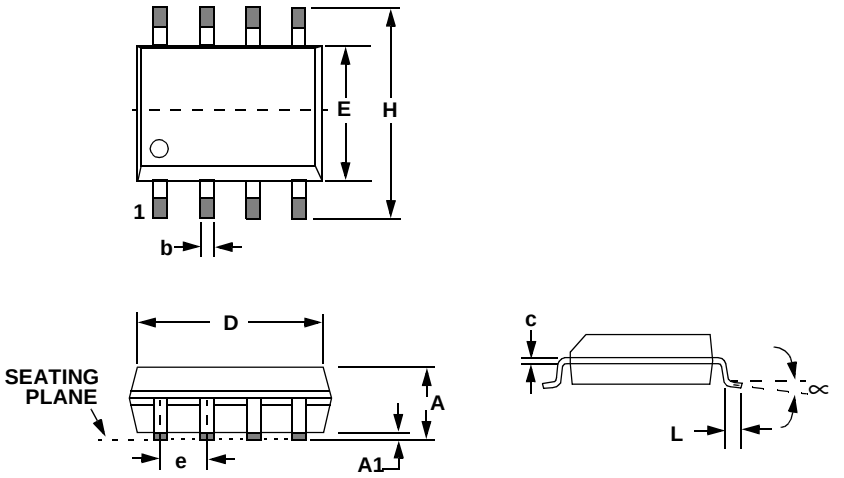
CS4330-BS ⇒ CS4339-BS

CS4331-BS ⇒ CS4334-BS

CS4333-BS ⇒ CS4338-BS

PACKAGE DIMENSIONS

8L SOIC (150 MIL BODY) PACKAGE DRAWING



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.013	0.020	0.33	0.51
C	0.007	0.010	0.19	0.25
D	0.189	0.197	4.80	5.00
E	0.150	0.157	3.80	4.00
e	0.040	0.060	1.02	1.52
H	0.228	0.244	5.80	6.20
L	0.016	0.050	0.40	1.27
∝	0°	8°	0°	8°

JEDEC # : MS-012

• Notes •

A DIVISION OF CIRRUS LOGIC

CDB4334/8/9

Evaluation Board for CS4334/8/9 Family of Products

Features

- Demonstrates recommended layout and grounding arrangements
- CS8414 Receives AES/EBU, S/PDIF, & EIAJ-340 Compatible Digital Audio
- Digital and Analog Patch Areas
- Requires only a digital signal source and power supplies for a complete Digital-to-Analog-Converter system

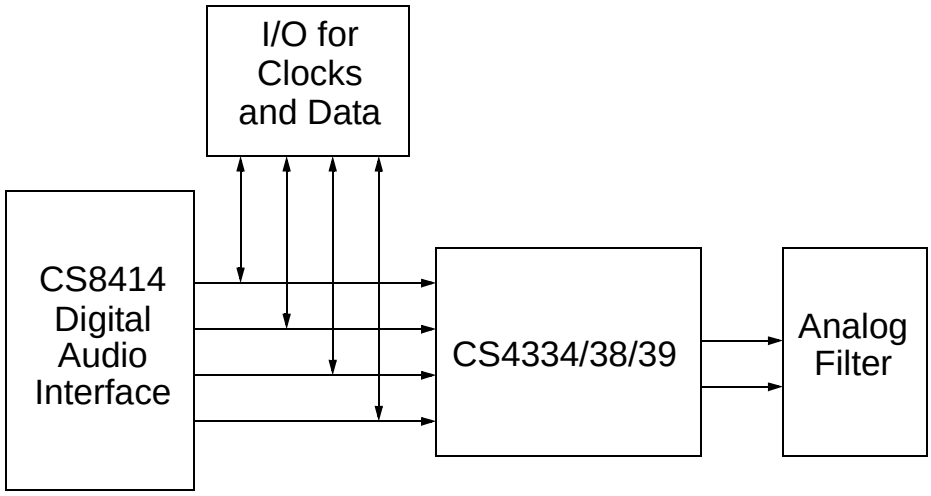
Description

The CDB4334/8/9 evaluation board is an excellent means for quickly evaluating the CS4334/8/9 family of 24-bit, stereo D/A converters. Evaluation requires an analog signal analyzer, a digital signal source and a power supply. Analog outputs are provided via RCA connectors for both channels.

The CS8414 digital audio receiver I.C. provides the system timing necessary to operate the Digital-to-Analog converters and will accept AES/EBU, S/PDIF, and EIAJ-340 compatible audio data. The evaluation board may also be configured to accept external timing signals for operation in a user application during system development.

ORDERING INFORMATION

CDB4334, CDB4338, CDB4339



Preliminary Product Information | This document contains information for a new product. Cirrus Logic reserves the right to modify this product without notice.

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CDB4334/8/9 SYSTEM OVERVIEW

The CDB4334/8/9 evaluation board is an excellent means of quickly evaluating the CS4334/8/9. The CS8414 digital audio interface receiver provides an easy interface to digital audio signal sources including the majority of digital audio test equipment. The evaluation board also allows the user to supply clocks and data through a 10-pin header for system development.

The CDB4334/8/9 schematic has been partitioned into 7 schematics shown in Figures 2 through 8. Each partitioned schematic is represented in the system diagram shown in Figure 1. Notice that the the system diagram also includes the interconnections between the partitioned schematics.

The CS8414 does not support a compatible data format for the CS4335, CS4336 or CS4337. As a result, an evaluation board is not available for these devices. However, the evaluation board does allow external generation of clocks and data, bypassing the CS8414, and will support the CS4335/36/37 in this configuration.

CS4334/8/9 DIGITAL TO ANALOG CONVERTER

A description of the CS4334/5/6/7/8/9 is included in the CS4334/5/6/7/8/9 data sheet.

CS8414 DIGITAL AUDIO RECEIVER

The system receives and decodes the standard S/PDIF data format using a CS8414 Digital Audio Receiver, Figure 5. The outputs of the CS8414 include a serial bit clock, serial data, left-right clock (FSYNC), de-emphasis control and a 256 Fs master clock. The operation of the CS8414 and a discussion of the digital audio interface are included in the CS8414 Datasheet.

During normal operation, the CS8414 operates in the Channel Status mode where the LED's display channel status information for the channel selected by the CSLR/FCK jumper. This allows the CS8414 to decode the de-emphasis bit from the digital audio interface for control of the CS4334/8/9 de-emphasis filter.

When the Error Information Switch is activated, the CS8414 operates in the Error and Frequency information mode. The information displayed by the LED's can be decoded by consulting the CS8414 data sheet. It is likely that the de-emphasis control for the CS4334/8/9 will be erroneous and produce an incorrect audio output if the Error Information Switch is activated and the CS4334/8/9 is in the internal serial clock mode.

Encoded sample frequency information can be displayed provided a proper clock is being applied to the FCK pin of the CS8414. When an LED is lit, this indicates a "1" on the corresponding pin located on the CS8414. When an LED is off, this indicates a "0" on the corresponding pin. Neither the L or R option of CSLR/FCK should be selected if the FCK pin is being driven by a clock signal.

The evaluation board has been designed such that the input can be either optical or coax, Figure 6. However, both inputs can not be driven simultaneously.

CS8414 DATA FORMAT

The CS8414 data format can be set with jumpers M0, M1, M2, and M3, as described the CS8414 datasheet. The format selected must be compatible with the data format of the CS4334/8/9, shown in Figures 4-7 of the CS4334/8/9 datasheet. The default settings for M0-M3 on the evaluation board are given in Tables 2-4. The compatible data formats we have chosen for the CS8414 and CS4334/8/9 are:

CS8414 format 2 ; CS4334

CS8414 format 5 ; CS4338

CS8414 format 6 ; CS4339

ANALOG OUTPUT FILTER

The evaluation board includes a pair of single pole passive filters and a pair of 3-pole active filters. The passive filters are provided as an example for cost-sensitive desigins. The active filters demonstrate a higher performance alternative with better out-of-band noise rejection. The passive filters, Fig. 4, have a corner frequency of approximately 95 kHz with JP3 and JP6 installed and 190 kHz without JP3 and JP6. The 3-pole active filters are shown in Fig. 3. The output filter options are selected via the Left and Right Channel filter jumpers, Fig. 2.

INPUT/OUTPUT FOR CLOCKS AND DATA

The evaluation board has been designed to allow the interface to external systems via the 10-pin header, J9. This header allows the evaluation board to accept externally generated clocks and data. The schematic for the clock/data I/O is shown in Figure 10. The 74HC243 transceiver functions as an I/O buffer where jumpers HDR1-HDR6 determine if the transceiver operates as a transmitter or receiver. A transmit function is implemented with the HDR1-HDR6 jumpers in the 8414 position. LRCK, SDATA, and SCLK from the CS8414 will be outputs on J9. The transceiver operates as a receiver with jumpers HDR1-HDR6 in the EXTERNAL position. MCLK, LRCK, SDATA and SCLK on J9 become inputs.

GROUNDING AND POWER SUPPLY DECOUPLING

The CS4334/8/9 requires careful attention to power supply and grounding arrangements to optimize performance. Figure 9 shows CDB power arrangements. The CDB4334/8/9 ground plane is divided in a manner to control to digital return currents in order to minimize noise. The decoupling capacitors are located as close to the CS4334/8/9 as possible. Extensive use of ground plane fill on both the analog and digital sections of the evaluation board yield large reductions in radiated noise effects.

CONNECTOR	INPUT/OUTPUT	SIGNAL PRESENT
+5 V	input	+ 5 Volt power
GND	input	ground connection from power supply
Digital input	input	digital audio interface input via coax
Optical input	input	digital audio interface input via optical
Digital I/O	input/output	I/O for master, serial, left/right clocks and serial data
AOUTLA	output	left channel analog output with 3-pole active filter
AOUTRA	output	right channel analog output with 3-pole active filter
AOUTLP	output	left channel analog output with single-pole passive filter
AOUTRP	output	right channel analog output with single-pole passive filter

Table 1. System Connections

JUMPER	PURPOSE	POSITION	FUNCTION SELECTED
CSLR/FCK	Selects channel for CS8414 channel status information	HI LO	See CS8414 Datasheet for details
M0 M1 M2 M3	CS8414 mode selection	*Low *High *Low *Low	See CS8414 Datasheet for details
SCLK	Selects SCLK Mode	INT *EXT	Internal SCLK Mode External SCLK Mode
DEM_8414	Selects source of de-emphasis control	*8414 DEM	CS8414 de-emphasis De-emphasis input static high
HDR1-6	Selects source of clocks and audio data	*8414 EXT	Selects CS8414 as source Digital I/O header becomes an source
MCLK	Selects High-Rate or Base-Rate Modes	x1 ÷2	Selects Base Rate Mode Selects High Rate Mode
Left Channel Filter	Selects Active 3-pole or passive single-pole filter	Active Passive	Selects 3-pole active filter Selects Single-pole passive filter
Right Channel Filter	Selects Active 3-pole or passive single-pole filter	Active Passive	Selects 3-pole active filter Selects Single-pole passive filter

*Default setting from factory

Notes: The CS8414 data format requires the CS4334 to operate in the external serial clock mode.

Table 2. CDB4334 Jumper Selectable Options

JUMPER	PURPOSE	POSITION	FUNCTION SELECTED
CSLR/FCK	Selects channel for CS8414 channel status information	HI LO	See CS8414 Datasheet for details
M0 M1 M2 M3	CS8414 mode selection	*High *Low *High *Low	See CS8414 Datasheet for details
SCLK	Selects SCLK Mode	INT *EXT	Internal SCLK Mode External SCLK Mode
DEM_8414	Selects source of de-emphasis control	*8414 DEM	CS8414 de-emphasis De-emphasis input static high
HDR1-6	Selects source of clocks and audio data	*8414 EXT	Selects CS8414 as source Digital I/O header becomes an source
MCLK	Selects High-Rate or Base-Rate Modes	x1 ÷2	Selects Base Rate Mode Selects High Rate Mode
Left Channel Filter	Selects Active 3-pole or passive single-pole filter	Active Passive	Selects 3-pole active filter Selects Single-pole passive filter
Right Channel Filter	Selects Active 3-pole or passive single-pole filter	Active Passive	Selects 3-pole active filter Selects Single-pole passive filter

*Default setting from factory

Notes: The CS8414 data format requires the CS4338 to operate in the external serial clock mode.

Table 3. CDB4338 Jumper Selectable Options

JUMPER	PURPOSE	POSITION	FUNCTION SELECTED
CSLR/FCK	Selects channel for CS8414 channel status information	HI LO	See CS8414 Datasheet for details
M0 M1 M2 M3	CS8414 mode selection	*Low *High *High *Low	See CS8414 Datasheet for details
SCLK	Selects SCLK Mode	INT *EXT	Internal SCLK Mode External SCLK Mode
DEM_8414	Selects source of de-emphasis control	*8414 DEM	CS8414 de-emphasis De-emphasis input static high
HDR1-6	Selects source of clocks and audio data	*8414 EXT	Selects CS8414 as source Digital I/O header becomes an source
MCLK	Selects High-Rate or Base-Rate Modes	x1 ÷2	Selects Base Rate Mode Selects High Rate Mode
Left Channel Filter	Selects Active 3-pole or passive single-pole filter	Active Passive	Selects 3-pole active filter Selects Single-pole passive filter
Right Channel Filter	Selects Active 3-pole or passive single-pole filter	Active Passive	Selects 3-pole active filter Selects Single-pole passive filter

*Default setting from factory

Table 4. CDB4339 Jumper Selectable Options

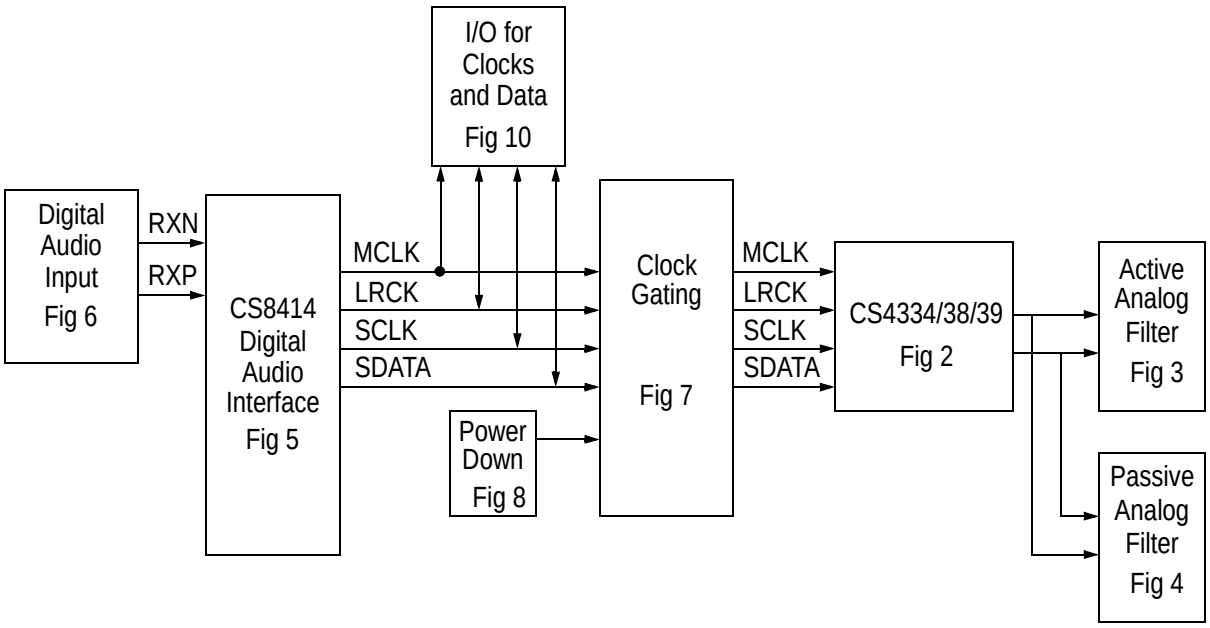


Figure 1. System Block Diagram and Signal Flow

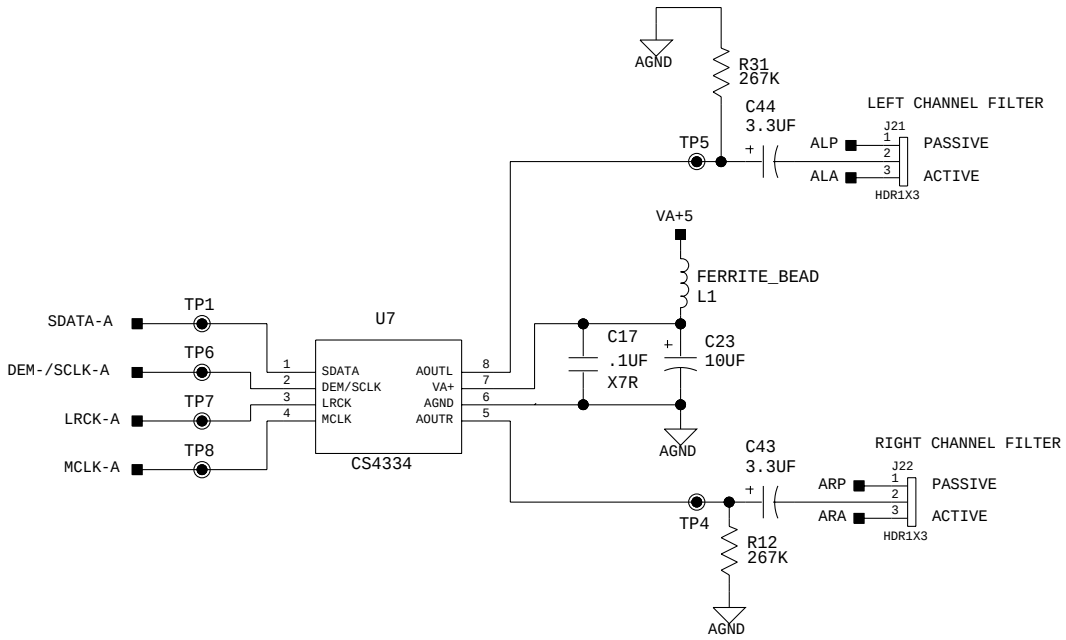


Figure 2. CS4334/5/6/7/8/9

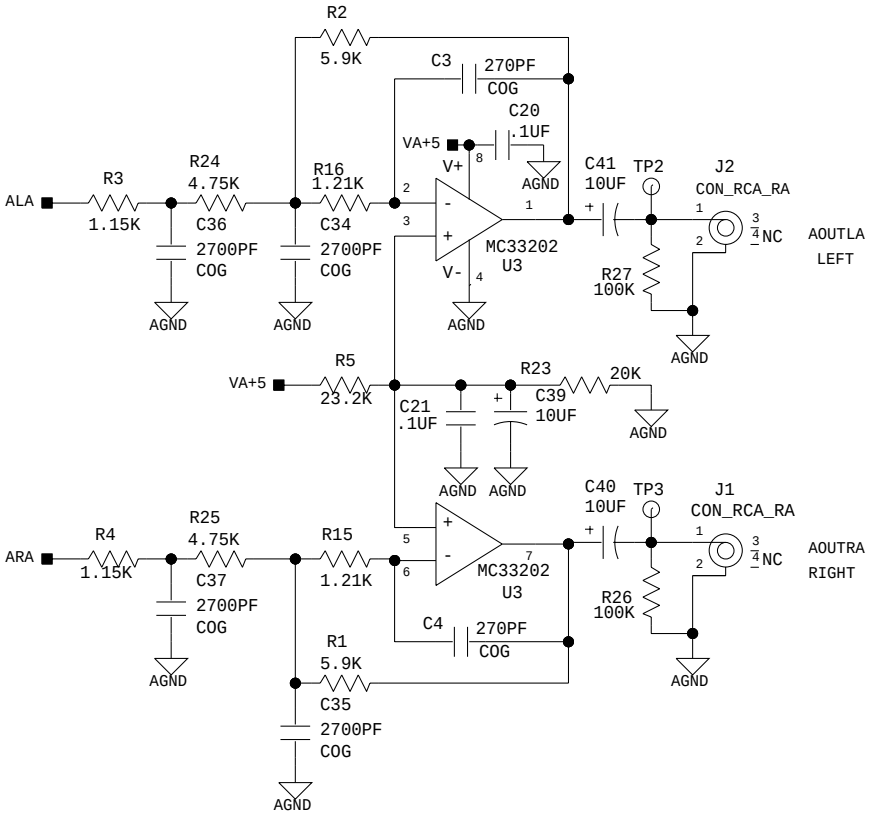


Figure 3. Analog Output Active Filter

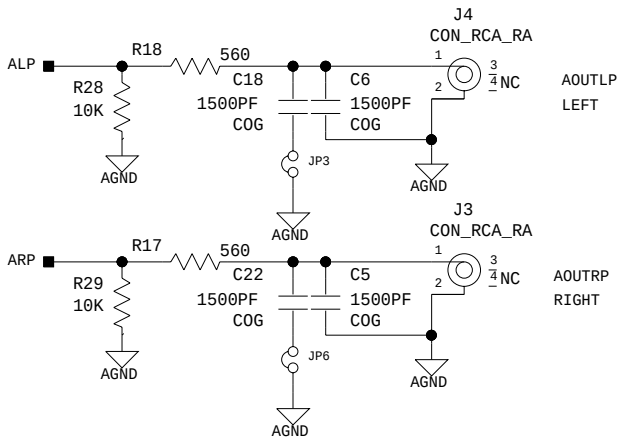


Figure 4. Analog Output Passive Filter

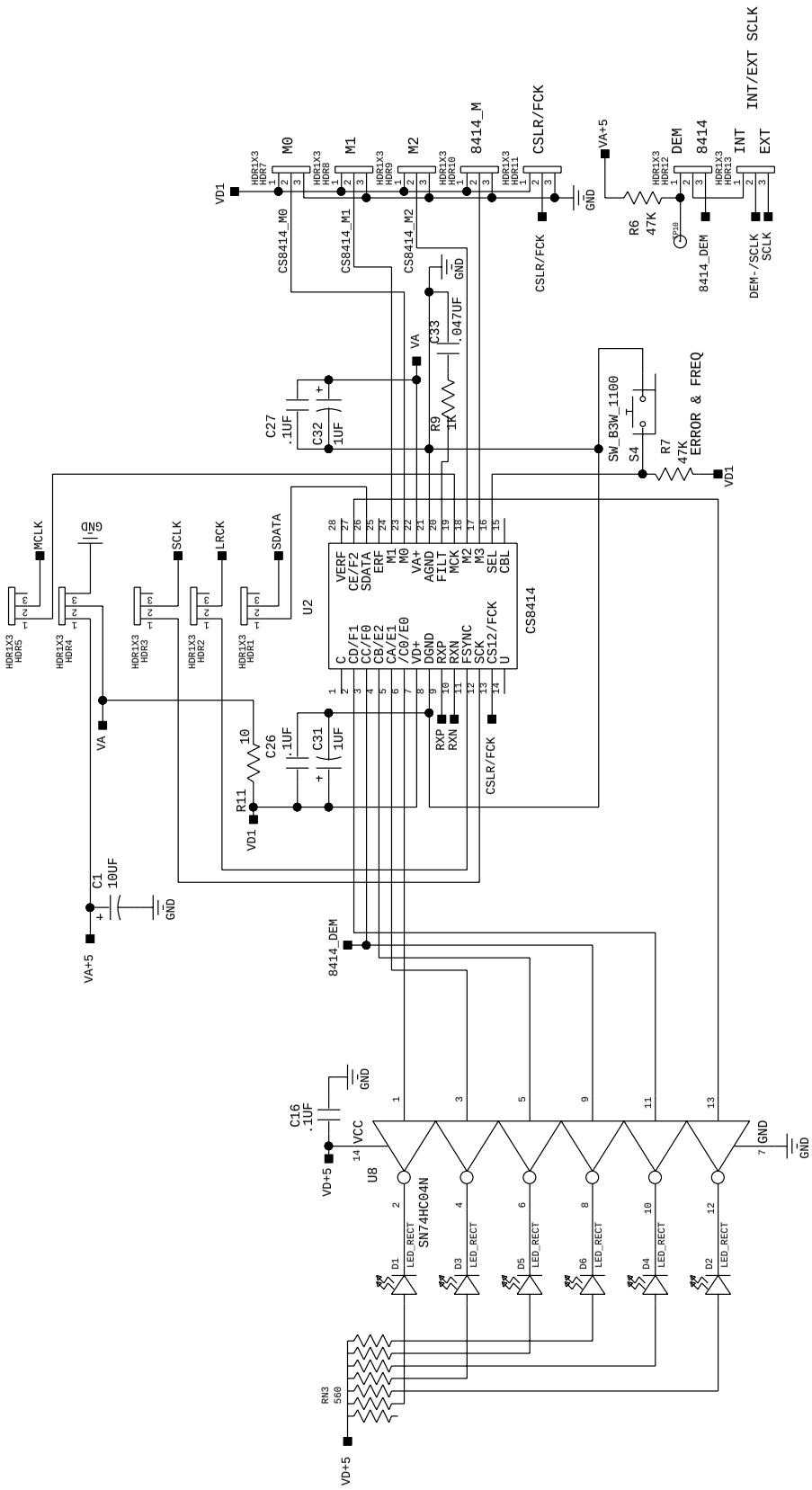


Figure 5. CS8414 Digital Audio Receiver Connections

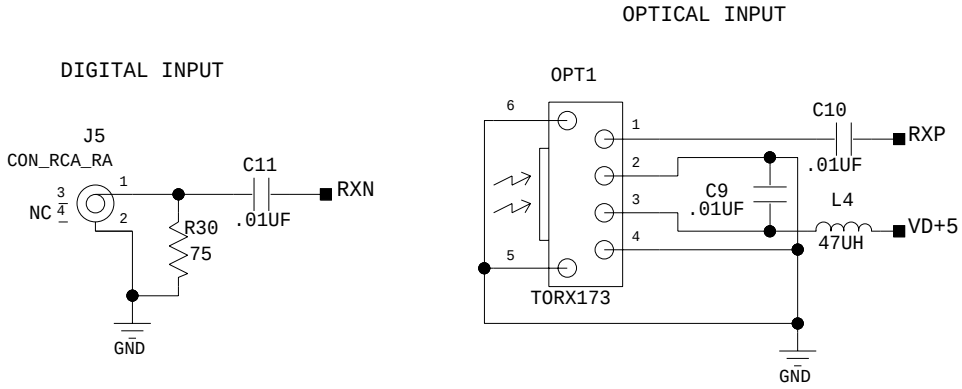


Figure 6. Digital Audio Inputs

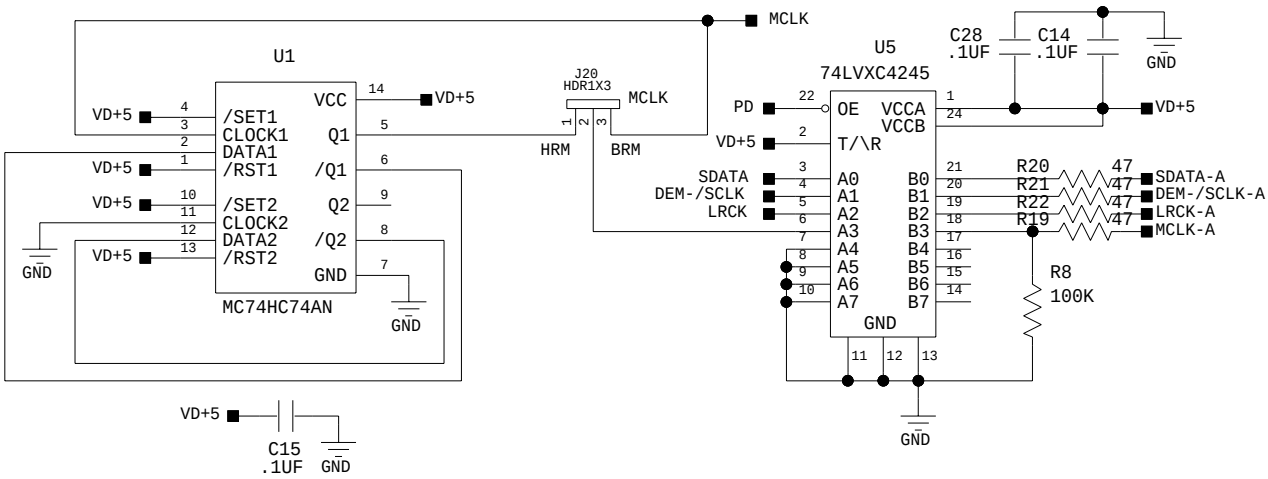


Figure 7. MCLK Divider and Clock Gating

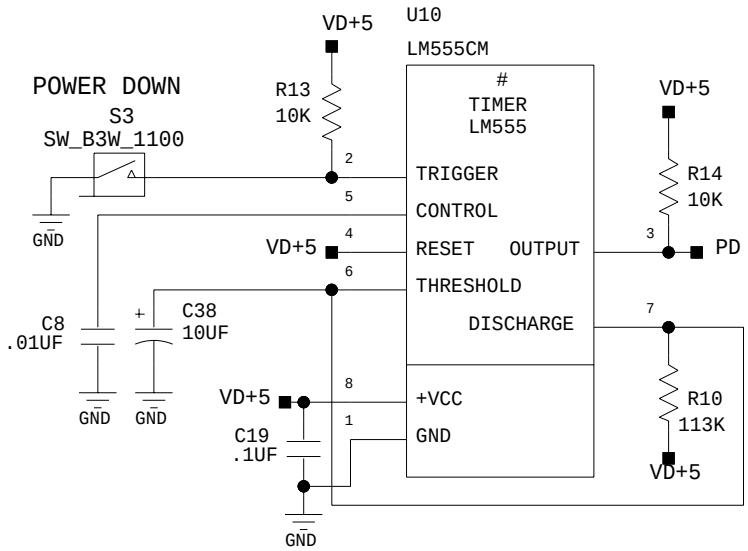


Figure 8. Power Down Circuitry

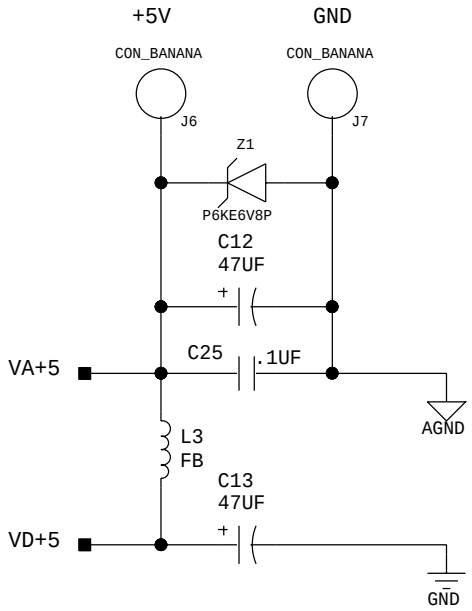


Figure 9. Power Supply

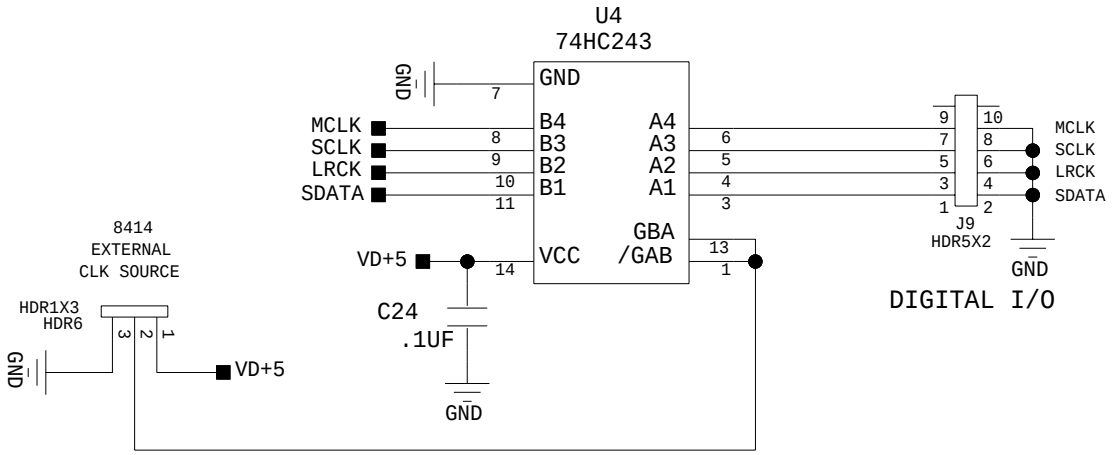


Figure 10. I/O for Clocks and Data

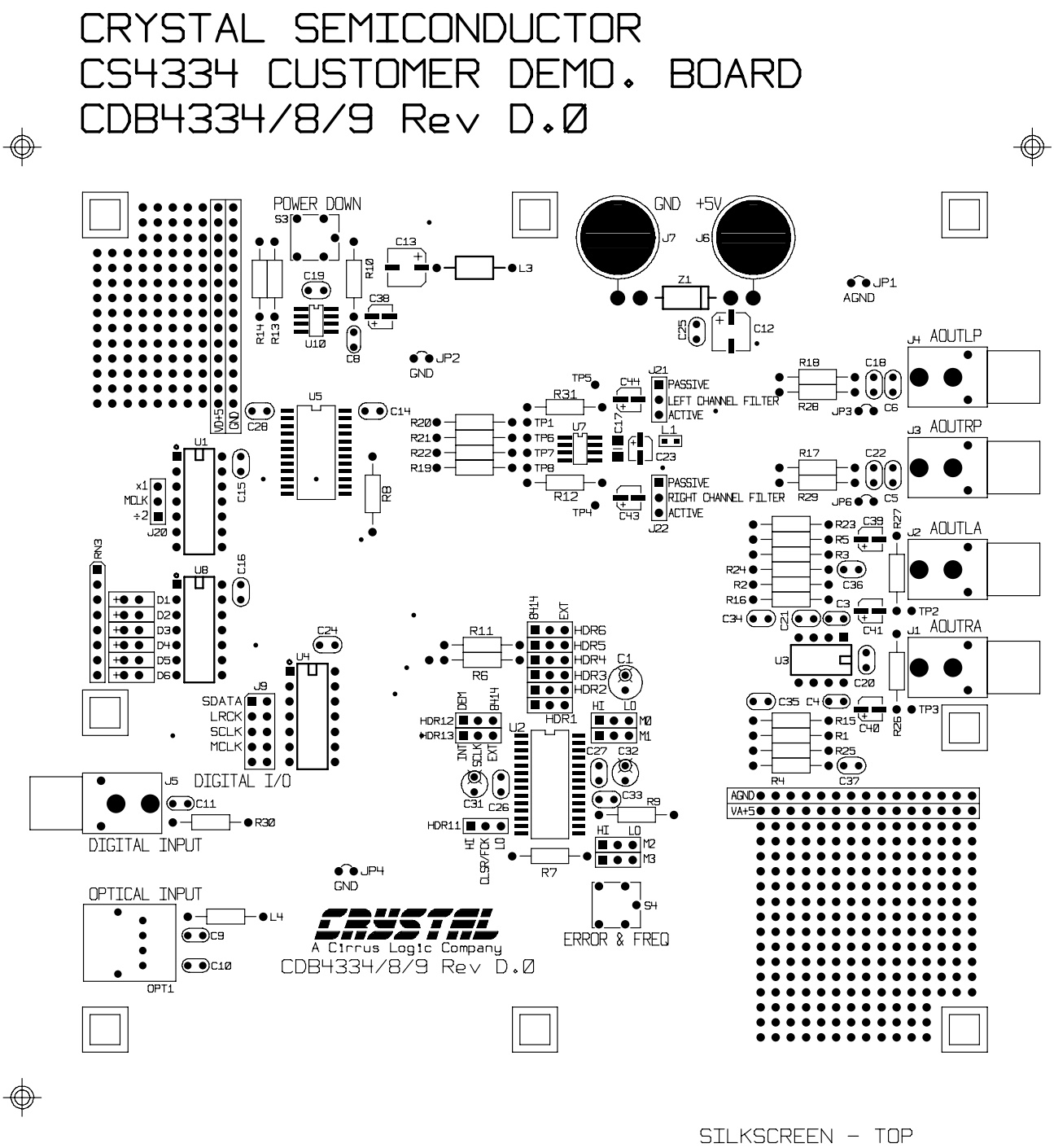
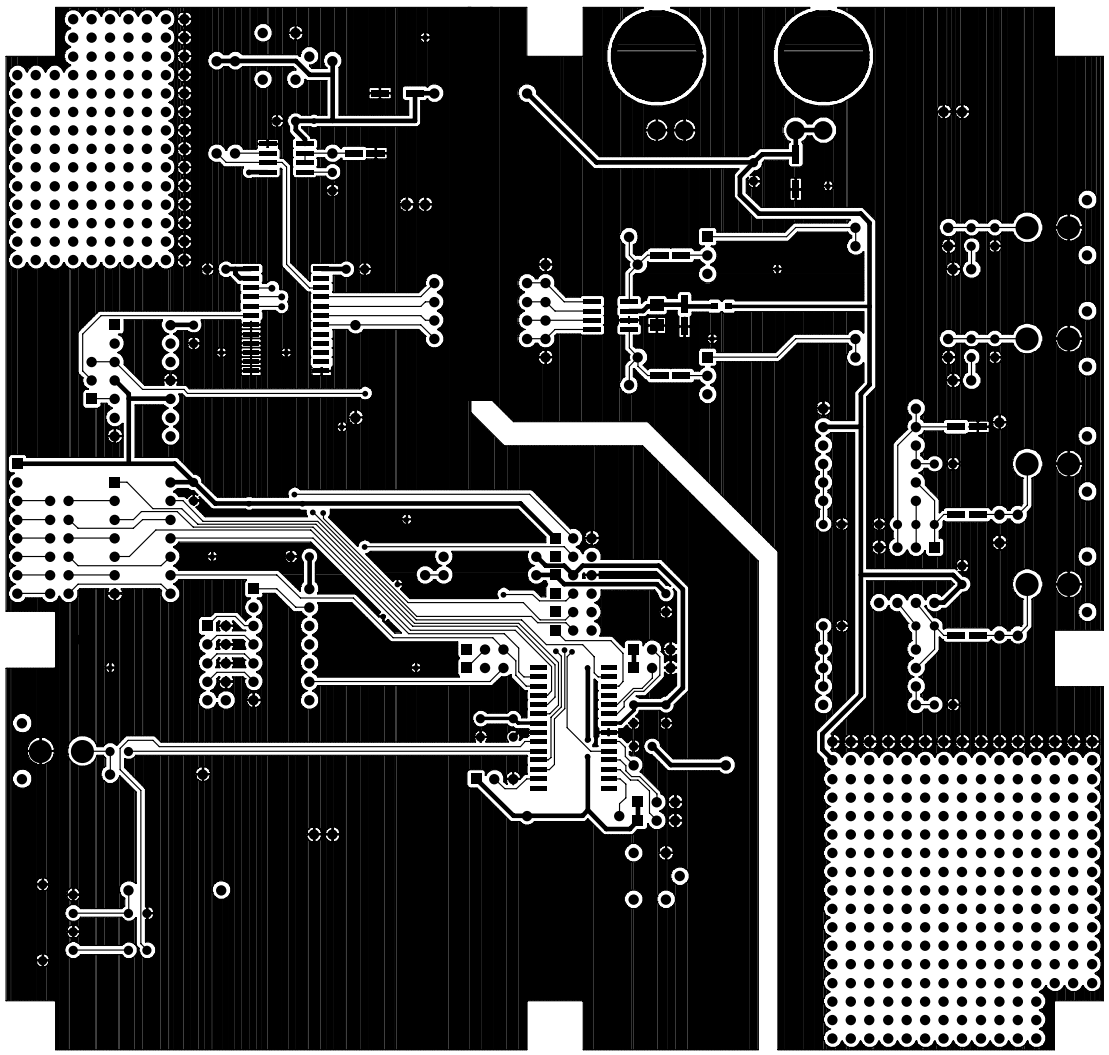


Figure 11. Silkscreen Top

CRYSTAL SEMICONDUCTOR
CS4334 CUSTOMER DEMO. BOARD
CDB4334/8/9 Rev D.0



TOP SIDE

Figure 12. Top Side

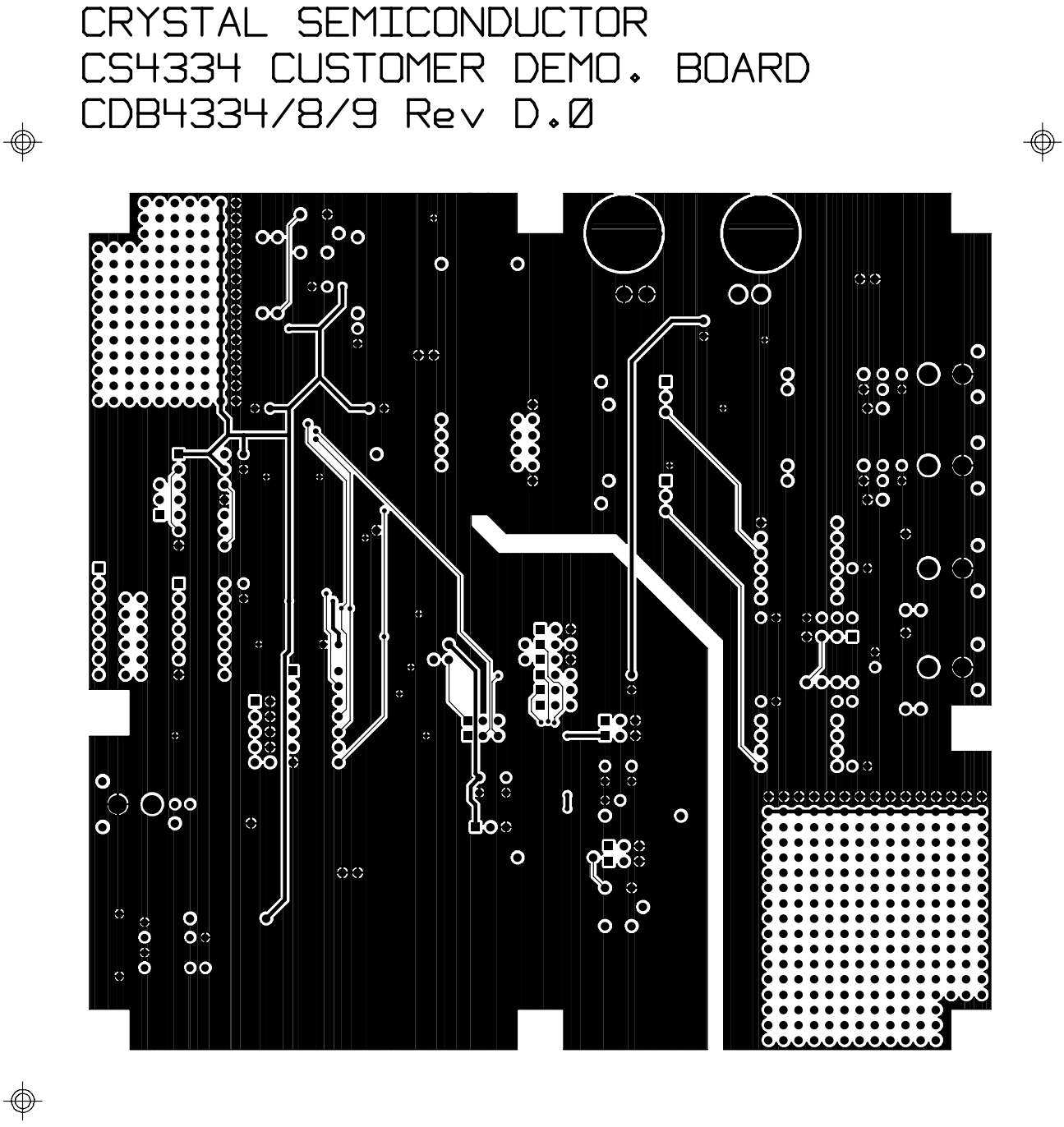


Figure 13. Bottom Side

• Notes •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